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METALIZING CERAMIC WITH PLATED COPPER ON THICK FILM TECHNOLOGY: PCTF®

Design Guidelines

These general parameters and specifications are intended to help manufacturing engineers and designers to create a circuit layout by utilizing the most effective metallization solutions while designing ceramic based products with plated copper on thick films (PTCF).

1. MANUFACTURING TECHNOLOGY FOR CERAMIC METALIZATION

PCTF technology is based on plating of copper on screen printable, thick film seed material, which is plated to the required thickness and configuration.
Basic rules developed for design and manufacturing of ceramic substrates with air fireable thick film materials, are applicable with some additions and modifications as described below.

2. PLATED COPPER LINE RESISTANCE

Plating thickness	Resistivity	Plating thickness	Resistivity
.001"	0.65 mΩ/sq.	.005"	0.14 mΩ/sq.
.002"	0.35 mΩ/sq.	.007"	0.10 mΩ/sq.
.003"	0.26 mΩ/sq.	.010"	0.06 mΩ/sq.

3. CERAMICS

3.1 Alumina (Al_2O_3)
Purity: 96% typical (other grades available on request).
Thickness: .005” - .100”
Available ceramic active area: 4.8” by 6.6” max. (as a function of thickness).
3.2 Beryllium Oxide (BeO)
Purity: 99.5%
Thickness: .010” - .040”
Available ceramic useful area: 4.0” by 4.0” max. (as a function of thickness).
3.3 Aluminum Nitride (AlN): Consult the factory for details.
3.4 General: Ceramic may be lapped or polished to meet specific requirements.

4. ASSEMBLY METHODS

4.1 Wire bonding with Gold and Aluminum wires.
4.2 Soldering using standard reflow techniques.
4.3 High temperature die attach and brazing.
4.4 Epoxy die attach.

5. METALIZATION SCHEMES

We use air fireable thick film materials as is (unplated) or in combination with plating to provide desired circuit pattern and surface finish appropriate for applicable assembly methods.

5.1 Thick film metallization: gold, platinum gold, silver, palladium silver and platinum silver.
5.2 Silver plated with copper, nickel and gold.
5.3 Silver plated with nickel and gold – AgENIG™.
5.4 Silver plated with copper, nickel, palladium and gold.
5.5 Silver plated with nickel, palladium and gold ENEP^{IG}.
5.6 Silver plated with copper, nickel and tin.

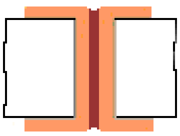
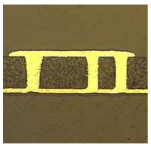
6. METALLIZATION THICKNESS

6.1 Printed thick films	Thickness:	5 – 40 microns.
6.2 Plated copper: MIL-C-14550.	Thickness:	.0005” - .010”
6.3 Nickel: Electrolytic QQN-290 Class 2.	Thickness:	100 - 250µ” typical.
6.4 Nickel: Autocatalytic MIL C 26074.	Thickness:	100 - 250µ” typical.
6.5 Gold: MIL-G-45204 Type III Grade A.	Thickness:	2 - 100µ” typical.
6.6 Immersion gold:	Thickness:	1 - 5µ” typical.
6.7 Tin:	Thickness:	200µ” typical, up to .003” available
6.8 Electroless palladium	Thickness:	4-16µ” typical

7. PLATED THROUGH HOLES, SOLID VIAS and CASTELLATIONS

7.1 Printed and Plated Through Holes provide reliable electrical connection between front and back of the ceramic substrates.

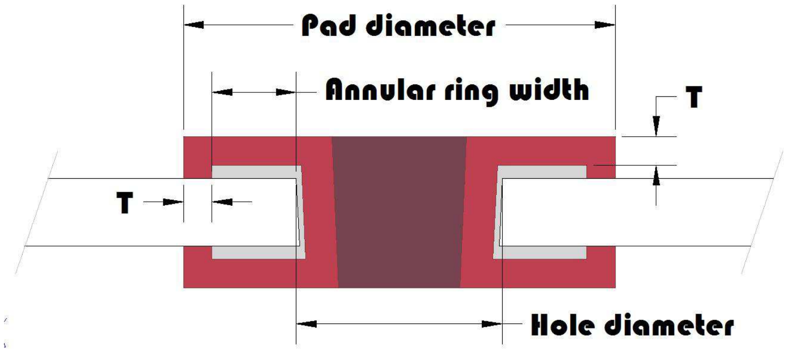
Visual representation of three available front–to-back interconnect techniques

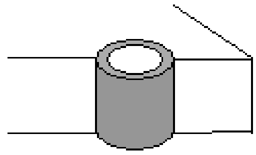
Plated Through Hole	Solid Plugged Via	Plated Castellation
		
Plated Copper Through Holes ensure a higher current carrying capacity, low loss RF signal and ground interconnections.	Solid plugged via holes are fully hermetic, withstand gross and fine leak test (10^{-8} atm cc/s). Plugged via holes provide excellent thermal and electrical signal and ground interconnections.	Plated Castellations / Wraparound provide for a reliable direct PCB attach / for SMT chip carriers and packages.

7.2 Solid Plugged Vias provide hermetic, high thermal and electrical conductivity connections.
7.3 Wraparounds (Castellations) provide cost effective, reliable SMT leadless connection for a direct PCB mounting.

7.4 Standard Dimensions for Plated Through Hole, Solid Plugged Via and Plated Castellation are listed below.

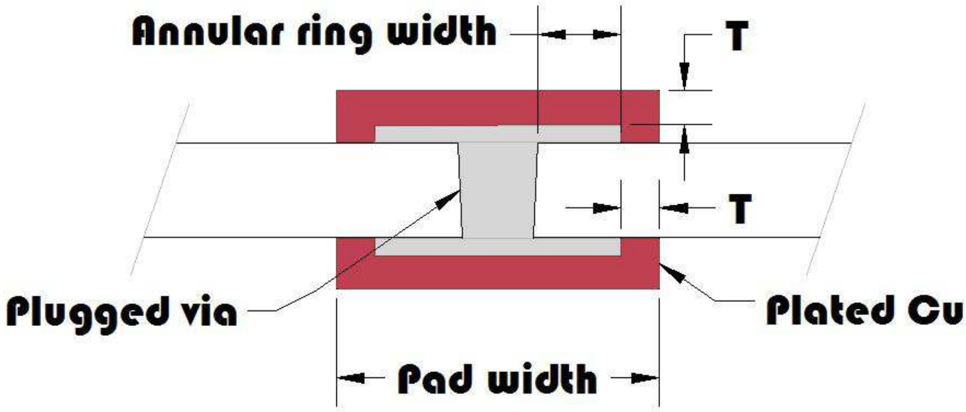
7.4.1 Plated Through Hole
Pad size for Plated Through Hole: Hole Diameter + (.010") Double Width of Annular Ring"+ Double Plated Thickness



Ceramic thickness	Through Hole Diameter	
.010" - .025"	.007"- .020"	
.025" - .040"	.009" - .030"	
.040" +	Consult Factory	

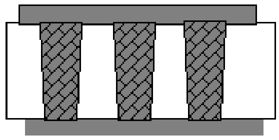
7.4.2 Solid Plugged Via
To ensure a reliable connection between plugged via and a metallization a minimum annular ring around the circumference of the plugged via hole should be as listed below:

- Standard annular ring width: .007" from each side minimum
- Premium annular ring width: .004" from each side minimum



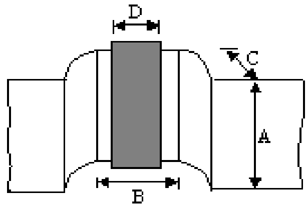
See par. 9.2 for hermetic via design rules.

Ceramic thickness	Standard	Maximum
.010”	.004” - .008”	.008”
.015”	.005” - .010”	.010”
.020”	.007: - .015”	.020”
.025’	.008” - .015”	.025”
.030”	.010” - .015”	.025”
.040”	.010” - .015”	.025”



7.4.3 Plated Castellation

Ceramic Thickness - A	Castellation Width – B, minimum	Castellation Depth – C, minimum	Metallization Width – D, Minimum. *
.040”	.040”	.006”	.025”
.025”	.030”	.005”	.020”
.020”	.030”	.005”	.020”
.015”	.026”	.005”	.018”



* Maximum metallization width equals castellation width minus .008”

Dmax=B-.008”.

7.5 Typical Through Hole Resistance values are listed below.

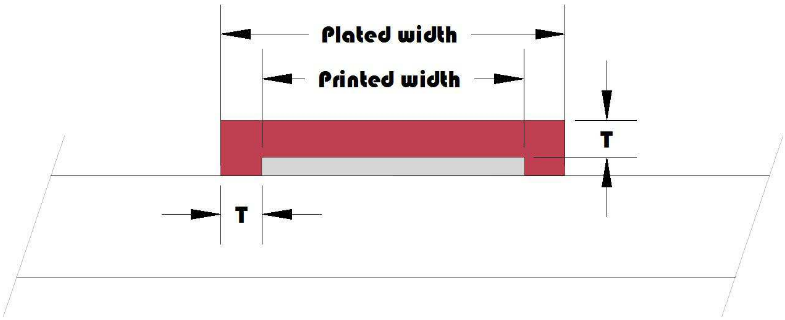
7.5.1	Typical Plated Through Hole Resistance		
	Ceramic thickness	Through Hole Diameter	Resistance (mΩ)
	.015”	.008”	0.40
	.025”	.010”	0.52
	.040”	.012’	0.70

7.5.2	Typical Plugged Via Hole Resistance		
	Ceramic thickness	Plugged Via Diameter	Resistance (mΩ)
	.010”	.005”	0.50
	.015”	.008”	0.42
	.020”	.010”	0.38
	.025”	.010”	0.47

7.5.3	Thermal conductivity of Plugged Via	
	Material	Thermal Conductivity W/°CxM
	PCTF: Ag + Cu	> 200
	Au	65

8. LAYOUT DESIGN RECOMMENDATIONS

8.1 To prepare the layout for plated copper technology, the required line width of the finished pattern must be scaled down for printing to accommodate lateral line growth during plating. The factor used for scaling down is defined by the required plating thickness. Width of the plated line is calculated as follows: Printed Line Width + Double Plated Thickness.

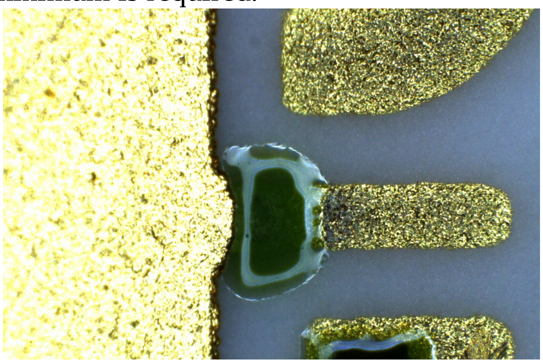


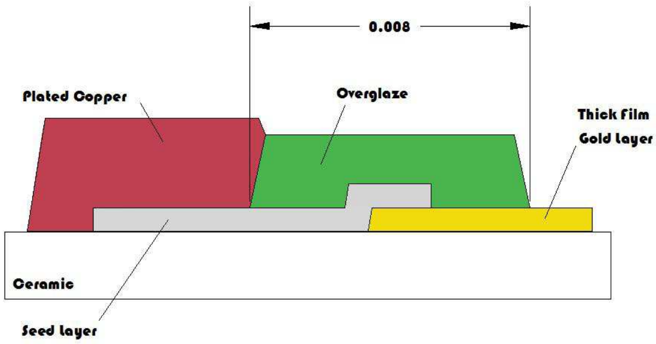
8.1.1 Minimum Line/Space dimensions for plated copper as a function of plating thickness are defined in table below:

Copper Thickness	Line/Space printed - before plating (typical)	Minimum Line/Space plated (typical)
.0005"	.005"/.006"	.006"/ .005"
.001"	.005"/.007'	.007"/ .005"
.002"	.006'/.010"	.010"/ .006"
.003"	.006'/.014"	.012"/ .008"
.004"	.008"/.018"	.016"/ .010"
.005"	.008"/.022"	.018"/ .012"
>.005"	Consult the factory	Consult the factory

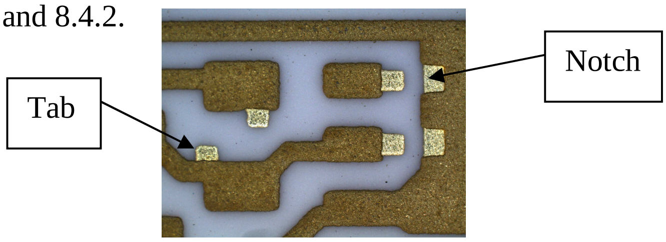
8.1.2 Minimum Line/Space dimensions can be reduced with special processing. Consult factory for details.

8.2 When plated copper pad and thick film line form continuous conductive path, the interface of .008" minimum is required.





8.3 Plating interconnects requirements:
PCTF technology requires to interconnect a stand-alone (electrically isolated) lines and/or pads to provide the connections required for electroplating. The most common ways are described in the paragraphs 8.4.1 and 8.4.2.



8.3.1. Tab: Attach small island of metal to stand alone line and/or pad. Tab may be either plated or unplated. Typical tab size: .010” by .015”.

8.3.2 Notch: Create small island of metal nested into stand-alone line and/or pad. Notch may be either plated or unplated. Typical notch size: .020” by .015”.

8.4 When designing RF-circuits include “Tabs” and “Notches” during simulation stage. Consult factory for details.

8.5 With special processing metallization can be copper plated without using “Tabs” or “Notches” – consult factory for details

8.6 Design limitations for circuits with PCTF Metallization Technology:

	Printed Thick Films		Plated Thick Films	
Item	Standard (inches)	Minimum (inches)	Standard (inches)	Minimum (inches}
Conductor Width	.010	.005	See table in 8.1	See table in 8.1
Conductor Spacing	.010	.005	See table in 8.1	See table in 8.1
Conductor to Glass Encapsulant Spacing	.006	.004	.006	.004
Conductor to Ceramic Pull Back *	.010	.003	.010	.005
Resistor Length (active area)**	.020	.010	.020	.010
Resistor Width (active area)**	.020	.010	.020	.010
Resistor/Conductor Overlap	.010	005	.010	005
Resistor/Glass Overlap Encapsulant	.010	.005	.010	.005
Glass Encapsulant Width	.008	.005	.008	.005
Wire bonding pad size (directly on ceramic)***	.008	.005	15	10
Wire bonding pad size (over plugged via)***	N/A	N/A	15	10

* Special processing allows to create “ZERO PULL BACK METALLIZATION”. See design guide lines for laser diode submounts.

** See par. 8.10 for more details.

*** Wire bonding pad size for plated thick films depends on copper thickness. Consult factory for details.

8.7 Multilayer structures can be achieved by combining thick film and plated copper technology. This method is often used when power and logic combined on the same substrate. Number of metal layers: up to 4 per each side of the ceramic. For Multilayer Thick Films all standard rules apply with some additions/exceptions as listed below.

Item	Standard (inches)	Minimum (inches)
Max Ceramic Panel	4x4	-
Dielectric Via size (Preferable square shape)	.010	.007
Conductor to Via Spacing	.010	.010

8.8 For Etched Thick Films all the above applies with smaller line/space dimensions and tighter tolerances added as listed below.

Item	Standard (inches)	Minimum (inches)	Tolerance (standard)	Tolerance (minimum)
Conductor Width	0.002	0.001	0.0002	0.0001
Conductor Spacing	0.002	0.001	0.0002	0.0001

8.9 To prevent solder from spreading into the areas adjacent to the solder pads, insulator is printed over the plated copper or thick film layers before plating takes place. Solder dams may be substituted by Liquid Photo Imageable mask for circuits with a higher density.

8.10 Standard resistor characteristics are described in the table below.*

Sheet Resistivity per square	.1Ω	1Ω	10Ω	100Ω	1KΩ	10KΩ	100KΩ	1MΩ
TCR (ppm/°C) Typical	350	150	100	100	100	100	100	100
Standard Working Voltage (V/Mil)		0.02	0.07	0.2	0.7	2.0	2.0	4.0
Maximum Rated Power Dissipation (W/ sq.in)		100 - 200	100 - 200	100 - 200	100 - 200	100 - 200	100 - 200	100 - 200

* Characteristics for resistor materials above 1MΩ per square are available on request.

8.10.1 Standard air fireable thick film resistors, from 100 mΩ up to 10MΩ per square. Giga ohm resistors are available on request.

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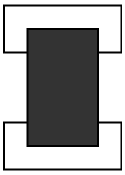
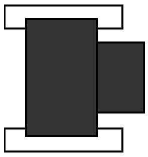
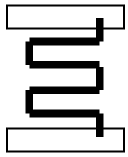
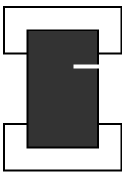
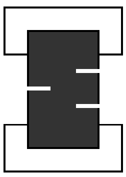
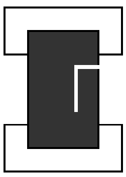
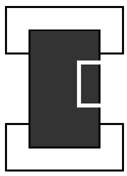
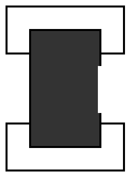
8.10.2 See table in par 8.6 for dimensions.
8.10.3 Power rating: consult factory for rating and required geometry.
8.10.4 Tolerances: ± 1% typical.
8.10.5 Matching: ± .5% typical.
8.10.6 TCR: 50- 200 ppm/°C typical.

Resistor Geometry		
Standard	Top Hat	Serpentine
		
Resistor/Termination overlap: .005” typical.		
Resistor Length: .010” min. Resistor Width .010” min.		
Covering with Over Glaze is recommended for improved resistor stability.		

8.10.7 To achieve the required tolerances resistors are trimmed by laser.
Laser Trim may reduce the active area of the resistor by 50% (Design resistor for 2X width if X is needed after trim). Basic trim configurations are outlined in the following table.

Standard Trim Available

Plunge	Serpentine	L - Cut	U- Cut	Scan - Cut
				
Tolerances after Laser Trim: from 1 % to 10%				
Matching tolerance between resistors up to 0.5%.				

9. HEMETIC PACKAGE (leaded and leadless): SPECIAL LAYOUT DESIGN CONSIDERATIONS
Hermeticity of a package is achieved by ensuring the hermeticity of both plugged via holes and hermetic sealing of ring frame to ceramic substrate.

9.1 Ring Frame Landing Area Width
Due to the necessity to ensure a proper solder fillet form the inner and outer sides of the ring frame the minimum dimensions required for solder fillets are listed below:

a) Standard: Minimum X = .010” from each side
b) Premium: Minimum X' = .008” from each side

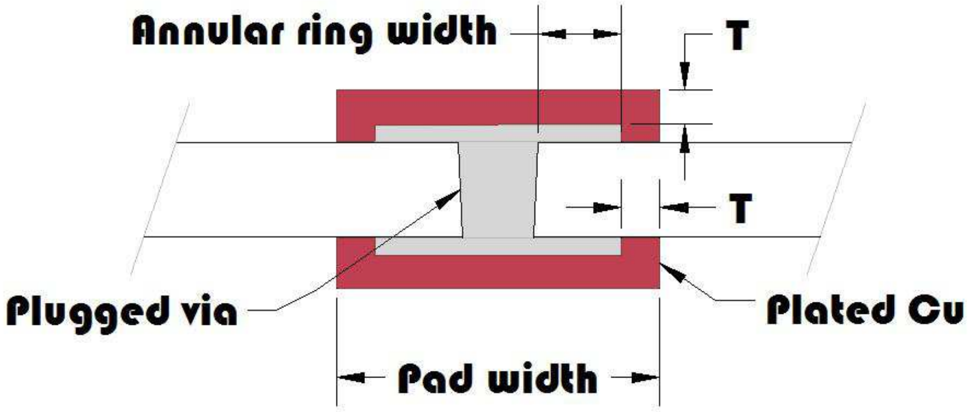
Following the above mentioned rule the landing area for the Ring Frame is calculated as follows:

Add	Ring Frame Wall Thickness
Add	Fillet width on both sides (2X or 2X')
=	Min Width of the Ring Frame landing area

9.2 **Plugged Via Metalization Diameter**

To ensure the hermeticity a minimum annular ring around the circumference of the plugged via hole should be as listed below:

- Standard annular ring width: .010" from each side minimum
- Premium annular ring width: .007" from each side minimum



Following the above mentioned rule the annular ring dimensions for the plugged via hole must be calculated as follows:

	Nominal diameter of the drilled hole
Add	10% of the ceramic thickness
Add	Annular ring width * 2
Add	Plating thickness
=	Min Diameter of the Annular Ring

10 CERAMIC PROCESSING

10.1 Standard holes size and tolerances:
Material thickness: .010" - .030", Min. Ø .006" ± .001"
.031" - .060", Min. Ø .010" ± .002"
Hole edge to hole edge distance must be typically equal or more than ceramic thickness.
Hole edge to ceramic edge: .020" typical, but not less than ceramic thickness.

10.2 Standard tolerances for laser machined features:

↓ From – To →	Scribe line center	Hole center	Machined edge
Scribed line center	±.001"	±.001"	±.001"
Scribed edge	±.003"	±.003"	±.003"
Machined edge	±.001"	±.001"	±.001"
As fired edge	±.010"	±.010"	±.010"

10.3 Scribe line tolerances:
Average depth: 40 - 60% of ceramic thickness.
Segment size tolerances after snapping: + .006” / - .002” typical.

10.4 Diced line tolerances:
Segment size tolerances after dicing: ± .001” typical.

11 TEMPERATURE RANGE

Operational: -55ºC to +150ºC.
Max. Assembly temperature: up to +420ºC.

12 FINISHED PART SUPPLY

12.1 Multiple parts arrays for automated assembly and testing.
12.2 Individual pieces singulated after laser scribing, laser machining or dicing.

13. QUALITY ASSURANCE

13.1 Qualification capabilities for MIL-STD 883, MIL – H-38534.
13.2 Quality system audited and approved for a number of commercial and military applications.